LISTING OF THE CLAIMS

The following listing of claims replaces all prior claim listings and versions in the application:

Claim 1 (Currently Amended)

A portable data storage device operable to write data with reference to a memory address mapping table configured to associate logical address regions with physical address regions, the portable data storage device including:

(i) a data interface for transferring data packets into and out of the portable data storage device;

(ii) an interface controller;

(iii) a master control unit; and

(iv) a NAND flash memory unit configured to incorporate the physical address regions;

the interface controller being operable to send data received through the data interface to the master control unit; and

the master control unit being operable:

to recognize a data packet received by the data interface as encoding one of a READ instruction indicating a logical address and a WRITE instruction indicating the logical address and data to be written;

upon receiving the READ instruction, to access the memory address mapping table, to read data from a first physical address of a first physical address region in the NAND flash memory unit, the first physical address corresponding, according to the memory address mapping table, to the logical address, and to transmit to the data interface one or more data packets including the data read; and

upon receiving the WRITE instruction, to determine, as a first determination, whether the first physical address is in an erased state, and

when a result of the first determination is affirmative, to write the data to be written to the first physical address, and

when the result of the first determination is negative:

(a) to modify the memory address mapping table in accordance with a block queue listing ~~one or more~~ a plurality of queuing physical address regions, the block queue comprising a pointer

to indicate a location of ~~to thereby associate~~ a second physical address ~~with the logical address, the second physical address belonging to a queuing physical address~~ region at a head of the block queue,

(b) to locate the second physical address region in accordance with the pointer to thereby associate ~~to write the data to be written to~~ the second physical address region with the logical address region containing the logical address, ~~and~~

(c) to write the data to be written to a physical address in the second physical address region, and

~~(c)~~ (d) to copy any data stored in other portions of ~~a~~ the first physical address region, originally associated with the logical address region containing the logical address, ~~designated by the first physical address~~ to corresponding locations of ~~a~~ the second physical address region ~~designated by the second physical address~~,

(e) to write the location of that first physical address region into the location to which the pointer points, and

(f) to move the pointer in a round-robin manner to indicate a location of a next one of the plurality of queuing physical address regions in ~~wherein following said modification of the memory address mapping table,~~ the block queue so that the location of ~~is modified to place~~ the first physical address is places, following said modification of the memory address mapping table, at ~~the~~ a rear of the block queue.

Claim 2 (Previously Presented)

The device according to claim 1, wherein the memory address mapping table is stored as mapping data in the NAND flash memory unit, the master control unit being operable to modify the mapping data upon modifying the memory address mapping table.

Claim 3 (Previously Presented)

The device according to claim 2, further comprising a memory control address unit operable, upon being initiated, to extract the mapping data from the NAND flash memory unit and to generate the memory address mapping table within RAM memory.

Claim 4 (Previously Presented)

The device according to claim 2, wherein a portion of the mapping data defining mapping between a respective physical address region and a logical address region is stored within the respective physical address region.

Claim 5 (Previously Presented)

The device according to claim 4, wherein the mapping data relating to the respective physical address region is stored in a control data storage sector of one or more pages of the respective physical address region.

Claim 6 (Canceled)

Claim 7 (Previously Presented)

The device according to claim 1, wherein the physical address regions listed on the block queue are in the erased state.

Claim 8 (Previously Presented)

The device according to claim 1, wherein the device further includes reserved physical address regions which cannot become associated with the logical address under an operation of the master control unit when modifying the memory address mapping table.

Claim 9 (Previously Presented)

The device according to claim 1, wherein each physical address region is a respective block of the NAND flash memory unit.

Claim 10 (Previously Presented)

The device according to claim 1, wherein the physical address regions comprise groups of blocks in the NAND flash memory unit, the groups being defined according to a grouping table.

Claim 11 (Previously Presented)

The device according to claim 10, wherein a majority of the groups of blocks is defined in the NAND flash memory unit according to a rule, and the grouping table defines groups positioned in the NAND flash memory unit according to exceptions to the rule.

Claim 12 (Previously Presented)

The device according to claim 11, wherein the memory address mapping table contains a flag for any logical address associated with one of the groups of blocks positioned according to the exceptions to the rule.

Claim 13 (Previously Presented)

The device according to claim 10, wherein the master control unit associates consecutively following logical addresses within a logical address region with respective pages in different ones of the blocks.

Claim 14 (Previously Presented)

The device according to claim 13, wherein the master control unit associates consecutive logical addresses into sets, each of the sets having a number of members equal to the number of blocks in each group, and for each given set the master control unit associates the logical addresses of the set with corresponding pages of the respective blocks.

Claim 15 (Previously Presented)

The device according to claim 1, wherein the master control unit is operable, in response to receiving a first WRITE instruction, to implement the first WRITE instruction only upon determining that, within a predefined period, a second WRITE instruction obeying a predefined similarity criterion is not received.

Claim 16 (Currently Amended)

A portable data storage device operable to write data with reference to a memory address mapping table configured to associate logical address regions with physical address regions, the portable data storage device including:

(i) a data interface for transferring data packets into and out of the portable data storage device;

(ii) an interface controller;

(iii) a master control unit; and

(iv) a NAND flash memory unit configured to incorporate the physical address regions;

the interface controller being operable to send data received through the data interface to the master control unit; and

the master control unit being operable:

to recognize a data packet received by the data interface as encoding one of a READ instruction indicating a logical address and a WRITE instruction indicating the logical address and data to be written;

upon receiving the READ instruction, to access the memory address mapping table, to read data from a first physical address in the NAND flash memory unit corresponding, according to the memory address mapping table, to the logical address, and to transmit to the data interface one or more data packets including the data read; and

upon receiving the WRITE instruction, to determine, as a first determination, whether the first physical address is in an erased state, and

when a result of the first determination is affirmative, to write the data to be written to the first physical address, and

when the result of the first determination is negative:

(a) to modify the memory address mapping table in accordance with a block queue listing one or more queuing physical address regions to thereby associate a second physical address with the logical address, the second physical address belonging to a queuing physical address region at a head of the block queue,

(b) to write the data to be written to the second physical address, and

(c) to copy any data stored in other portions of a first physical address region designated by the first physical address to corresponding locations of a second physical address region designated by the second physical address;

wherein the master control unit is operable, in response to receiving a first WRITE instruction, to implement the first WRITE instruction only upon determining that, within a predefined period, a second WRITE instruction obeying a predefined similarity criterion is not received; and

~~The device according to claim 15,~~ wherein following a modification of the memory address mapping table in relation to a first logical address, and prior to said copying of the data from the first physical address to the second physical address, said similarity criterion is whether the second WRITE instruction relates to a logical address corresponding to a location designated by the first logical address of the data to be copied, and when the similarity criterion is satisfied, aborting said copying operation and instead writing data specified by the second WRITE instruction to the second physical address.

Claim 17 (Previously Presented)

The device according to claim 15, wherein the master control unit is further operable to access a data cache and in response to the first WRITE instruction, and to write the data to the data cache, said similarity criterion being that the second WRITE instruction relates to the same logical address as the first WRITE instruction, and when the similarity criterion is satisfied, to write the data specified in the second WRITE instruction to the data cache.

Claim 18 (Previously Presented)

The device according to claim 15, wherein the master control unit is further operable to access a data cache and in response to the first WRITE instruction writes the data to the data cache when the first WRITE instruction relates to one or more selected logical addresses, said similarity criterion being that the second WRITE instruction relates to the same logical address as the first WRITE instruction, and when the similarity criterion is satisfied, to write the data specified in the second WRITE instruction to the data cache.

Claim 19 (Previously Presented)

The device according to claim 18, wherein the WRITE instruction relates to a plurality of said selected logical addresses.

Claim 20 (Previously Presented)

The device according to claim 18, further including a pattern recognition unit operable to recognize as a high frequency logical address a logical address encoded in WRITE instructions that is received with high frequency, and to set said high frequency logical address as said selected logical address.

Claim 21 (New)

A portable data storage device including:

(i) a data interface for transferring data packets into and out of the device,

(ii) an interface controller,

(iii) a master control unit, and

(iv) at least one NAND flash memory unit,

the interface controller being arranged to send data received through the interface to the master control unit, and

the master control unit being arranged to recognise certain data packets as encoding READ instructions and other data packets as encoding WRITE instructions;

(a) upon receiving a READ instruction indicating a logical address, to access a memory address mapping table which associates logical address regions within a logical memory space with respective first physical address regions within the memory unit, to read data from a physical address in the memory unit corresponding to the logical address according to the address mapping table, and to transmit to the data interface one or more data packets including the data which was read; and

(b) upon receiving a WRITE instruction indicating a logical address and data to be written to that logical address, to determine if the physical address corresponding to the logical address according to the memory address mapping table is in the erased state, and:

if so, to write the data to that physical address, or

if not, to modify the address mapping table to associate a second physical address region with the logical address region containing the logical address, to write the data to a physical address corresponding to the logical address according to the modified memory address mapping table, and to copy any data stored in other potions of the first physical address region to corresponding locations of the second physical address region;

wherein the master control unit is arranged, in response to receiving a first WRITE instruction, to implement the write instruction only upon determining that, within a predefined period, a second WRITE instruction is not received obeying a predefined similarity criterion; and

wherein following a modification of the memory address modification table in relation to a given logical address region, and prior to said copying of the data from the first physical address region to the new second address region, said criterion is whether the second WRITE instruction relates to a logical address corresponding to the location within the given logical

address region of the data to be copied, and in the case that such a WRITE instruction is received, aborting said copying operation and instead writing data specified by the second WRITE instruction to the location of the second physical address region.